ECE 322: BJT Lab #3 - Mini-Op Amp

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***Abstract* --** This lab is a continuation of the previous document entitled "ECE 322: BJT Lab #2 - Differential Amplifier Applications". This experiment takes the previously design differential amplifier stage and finds a fitting output stage to create a "mini op amp" circuit. Class A output stages were simulated using both BJT, MOSFET, and vacuum tube devices. This experiment then allows for better understand the fundamental differences in device characteristics when utilized as a voltage follower.

I. INTRODUCTION

This document is a continuation of a previous lab experiment whereby a differential amplifier was designed, built, and characterized. For this lab, the same differential amplifier design was utilized as a front-end to a "mini op amp". This op amp design includes an output stage to lower the output impedance and create a circuit similar to what one could find in a modern opamp integrated circuit. Though this design serves as a very crude type of opamp, it allowed for examination of output stage characteristics.

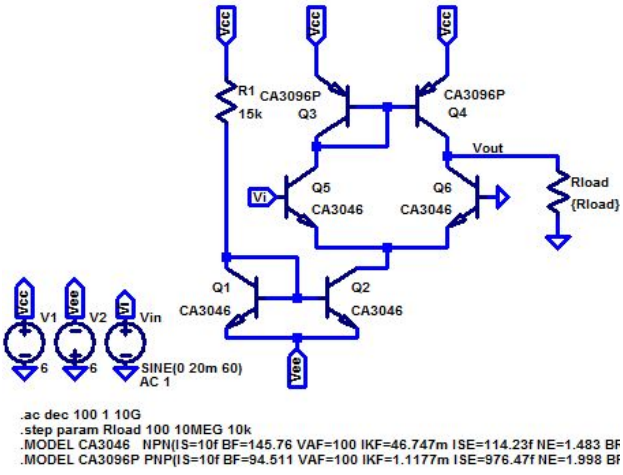
Output stages are typically used to deliver current to a load. It is most often desired to have a low output resistance in this case so that maximum power transfer can be achieved without losses. For this experiment, several different styles of output stages were simulated and examined. Ultimately, the more simple designs were chosen for the build process in order to examine the differences between various types of devices and how they function in this role.

II. PROCEDURE

Part A: Effects of High Output Impedance

This section builds on the differential amplifier circuit from the previous lab shown in **Figure 1**. It focuses on the effects of high output impedance by using LTspice to simulate a load resistor across the output terminals of the amplifier. An AC analysis was done to determine the effects of the loading resistor on the gain of the amplifier. The value of the loading resistor was stepped from 100 Ω to 10 MΩ as the frequency was increased from 1 Hz to 10 GHz.

***Figure 1**: Differential Amplifier Circuit*

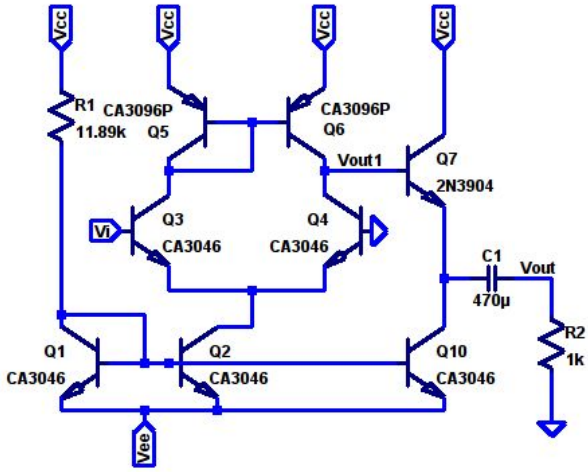


Part B: Output Stage - Design and Simulation

After taking a look at the effects of a loading resistor on the output of the differential amplifier circuit, several output stages were simulated using LTspice in order to determine how different configurations compared to one another and which might be best utilized in our design.

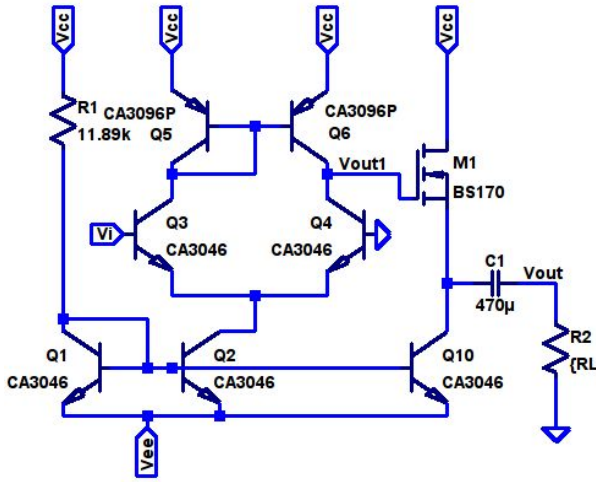
Output stages were examined for output impedance and effective power transfer to the load. The intended DC offset of the output stage was less than 100 mV. For the sake of simplicity, class A voltage follower output stages using both BJT and MOSFET devices like those shown in **Figure 2** and **Figure 3**.

***Figure 2**: Differential Amplifier with BJT Output Stage*



Lastly in this section, simulations were run in order to characterize the complete op amp circuit. Approximate hand calculations were also performed for comparison to the simulation. These calculations were also compared with the results from Part A.

***Figure 3**: Differential Amplifier with MOSFET Output*



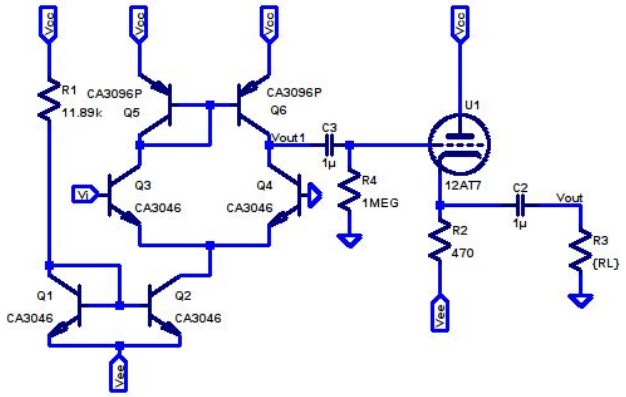
Part C: Mini Op Amp - Build and Test

With a number of designs simulated and calculated, this section involved making a selection, building the output stage for our amplifier, and making comparisons of the physical build to our simulated design. Measurements were made with a range of resistive loads in order to make these comparisons. The characterization the op amp circuit should provide a solid understanding of how the physical manifestation of these circuits compare.

Part D: Enhancing the Op Amp

For this section, the group was given the ability to choose a method for enhancing the op amp circuit. It was decided for this section to use an antiquated 12AT7 twin triode vacuum tube as an output stage in a voltage follower configuration. Given the design of this device, it doesn't lend itself to the efficiencies found in modern active devices. However, this device was chosen in order to better understand the operating characteristics of vacuum tubes at low voltages. This configuration is shown in **Figure 4**.

***Figure 4**: Differential Amplifier with Vacuum Tube Output*



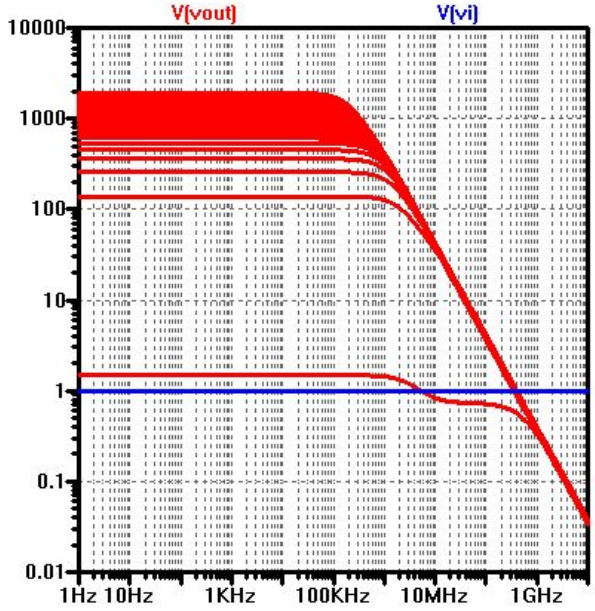
III. RESULTS

Part A: Effects of High Output Impedance

The LTspice simulations for this section provided useful for the considerations of the effects of output impedance

versus load impedance. **Figure 5** illustrates the effects of the gain of the amplifier with various resistive loads. From the figure, the lowest amount of gain can be seen with the 100 Ω load. At 10 kΩ, the mid-band gain is around 150 and steadily increases as the load resistance increases.

***Figure 5**: Differential Amplifier with Resistive Loads*



Part B: Output Stage - Design and Simulation

A BJT voltage follower was chosen as the first design. The first part of designing our output stage comes from looking at the output impedance of the differential amplifier stage by itself. From the previous report, it was determined that the current source delivered to the differential amplifier stage (I_{EE}) was to be ~1 mA. Using this approximate value, this current is split into the two halves of the circuit. Looking at the half that takes the output, that gives a current of 500 μA through Q6 and Q4. The gain in the differential amplifier can be calculated given the expression:

$$A_v = -g_m R_{L1} \qquad (1)$$

Since the active load of the PNP transistor has an output resistance (r_o) in parallel with the NPN high transistor, R_L is equal to these two resistances in parallel. From the CA3046 and CA3096 models, the Early voltage (V_A) is given at 100 V with a β of 100. Furthermore, the transconductance (g_m) for this circuit is approximately 20 mS. Thus, there is enough information to determine the output resistance of this stage.

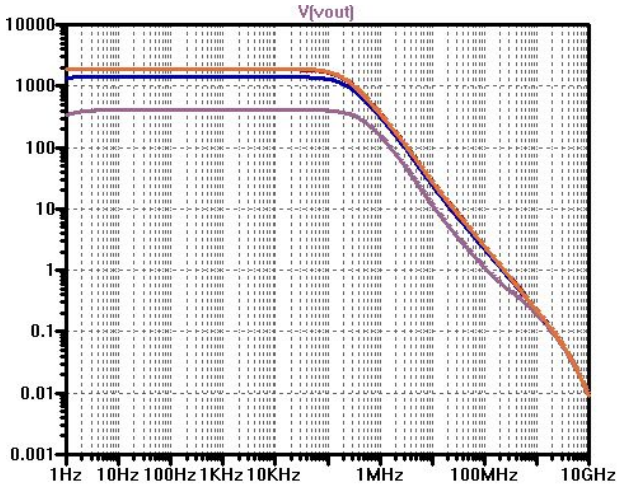
$$R_{out1} = R_{L1} = \left(\frac{100\ V}{500\ \mu A} \parallel \frac{100\ V}{500\ \mu A}\right) \approx 100\ k\Omega \qquad (2)$$

Starting now with a simple BJT voltage follower using a 2N3904, the output stage can be calculated using the following equation where β for this transistor is now 300.

$$R_{out2} = \frac{1}{g_m} + \frac{R_{L1}}{\beta} = 25\ \Omega + 333\ \Omega \approx 358\ \Omega \qquad (3)$$

Using the schematic shown in **Figure 2**, the resistive load of the entire amplifier is now stepped in 1 kΩ increments from 100 Ω to 1 MΩ. The AC analysis showing the gain of the amplifier in this configuration is shown in **Figure 6**.

***Figure 6**: AC Analysis BJT Output (100 Ω - 1 MΩ Load)*



Next, a MOSFET voltage follower was examined using a BS170 NMOS transistor. Due to the infinitely input resistance of the MOSFET, the formula for the output resistance is considerably simplified. Calculating g_m for the NMOS shown in **Figure 3** is done in the following manner.

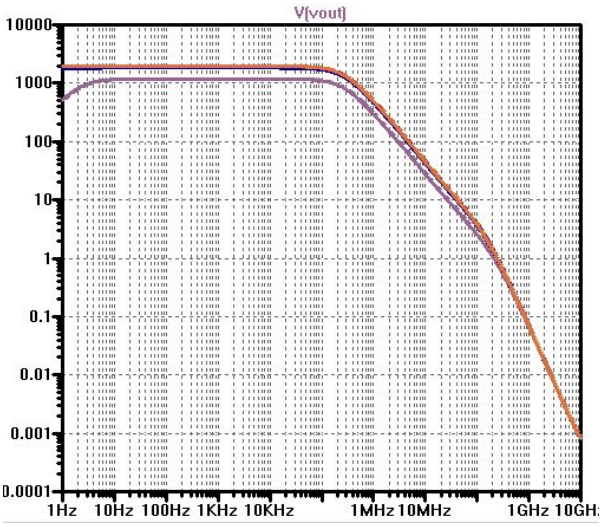
$$g_m = \sqrt{2K_nI_D} = \sqrt{2 * .1233 * 1\,mA} \approx 15\,mS \qquad (4)$$

For the BS170, the LTspice model gives a K_n of 0.1233 A/V^2. This gives a g_m of roughly 15 mS as shown in equation 4. Plugging this value into our formula, the output resistance for this stage is found.

$$R_{out} = \frac{1}{g_m} \approx 63.8\,\Omega \qquad (5)$$

Figure 7 shows a plot of the frequency response utilizing the NMOS output stage. The NMOS definitely shows some advantages in this arena over its BJT counterpart. With its considerably lower output resistance, there is much less of an affect on the gain of the overall amplifier.

***Figure 7**: AC Analysis NMOS Output (100 Ω - 1MΩ)*



Part C: Mini Op Amp - Build and Test

The first build for this section was the BJT output stage. **Figure 8** shows the actual build following the schematic shown in **Figure 2**. A 50 kΩ potentiometer was placed after the input signal to attempt to attenuate the 20 mV signal from the function generator. Since the expected gain of the amplifier was well above 1000, a much smaller input signal would be needed.

Figure 8: Circuit Build with BJT Output Stage

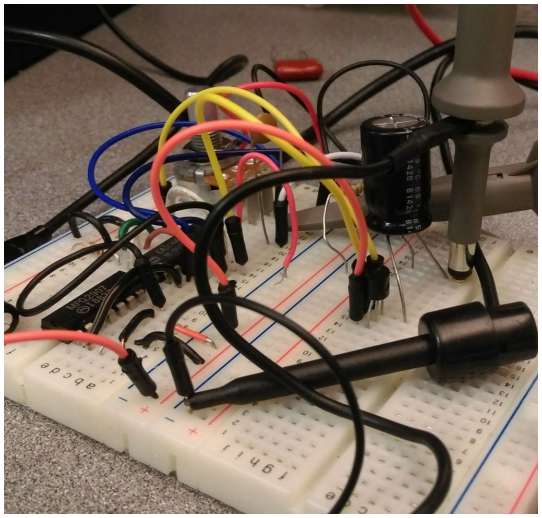


Figure 9 shows the input (on channel 1 in yellow) and output (channel 2 in blue) of the amplifier as captured on the oscilloscope. One thing to point out is that the measured input voltage is actually one tenth that value as measured with a digital multimeter. This is also measured with a 1 MΩ load.

***Figure 9**: Output of Build with BJT Output Stage*

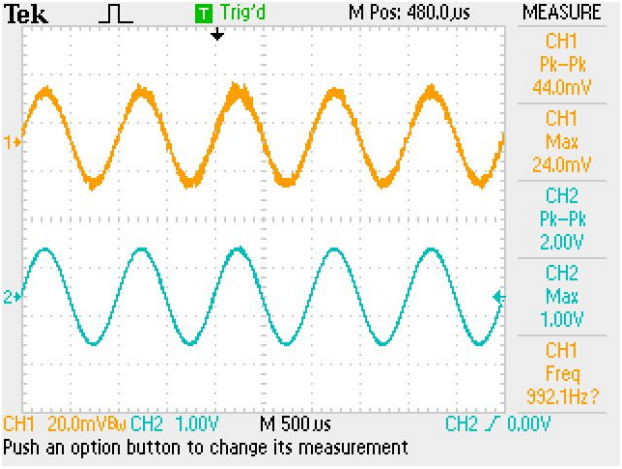


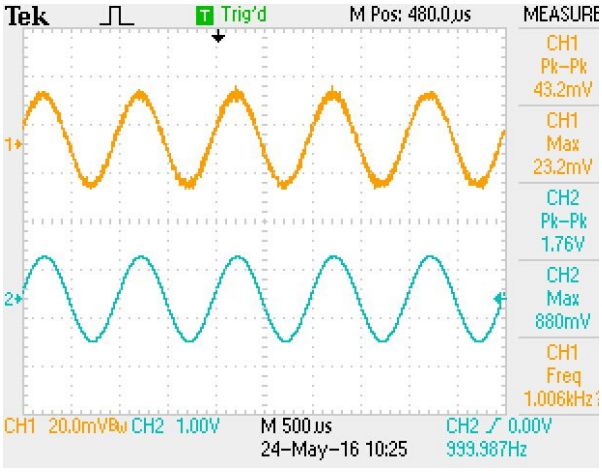
Figure 10 shows the input and output for the amplifier using the MOSFET output stage. The measurements were taken in a similar fashion as the BJT output stage. Here, we see a slight decrease in the output signal.

After the output signal was examined, the output resistance of each stage was measured as well. In order

to get a more accurate measurement of the output resistance, the following calculation was performed.

$$R_{OUT} = R_{LOAD}\left(\frac{V_{OPEN}}{V_{LOAD}} - 1\right) \quad (6)$$

***Figure 10**: Output of Build with MOSFET Output Stage*



Equation 6 allowed for the output resistance to be found by measuring the voltage on the output terminals with two different resistive loads. This method is arguably more effective than using additional components and was useful in illustrating the effects of the different loads. **Table 1** shows the measured, simulated, and expected specifications of the amplifier using a 1 MΩ load. The percent difference is calculated with respect to hand calculations.

***Table 1**: Amplifier Specification Comparison*

Param	Hand	LT	Build	% Diff
$A_{v\ BJT}$	2000	1929	1000	-50.0 %
$R_{in\ BJT}$	20 k	23 kΩ	24.2 kΩ	21.0 %
$R_{out\ BJT}$	358 Ω	461	34.4 Ω	-90.4 %
$A_{v\ NMOS}$	2000	1945	880	-56.0 %
$R_{in\ NMOS}$	20 k	23.2 kΩ	27.6 kΩ	38.0 %
$R_{out\ NMOS}$	63.8 Ω	92.2	104 Ω	63.0 %

Part D: Enhancing the Op Amp

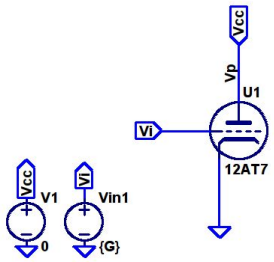
In order to utilize the vacuum tube for the output stage, it was necessary to repeat the steps in Part III in order to bias the device properly. This was somewhat different as vacuum tube characteristics heavily depend on the device's amplification factor. Fortunately, the amplification factor (μ) of a vacuum tube is one of the most stable parameters and is given in the datasheet as 60 for the 12AT7. It is also worth noting that the terminals for this device are the anode (similar to collector or drain), the grid (similar to base or gate), and the cathode (similar to emitter or source). The cathode is customarily noted by the letter, k, which will be seen in the coming equations.

In order to make any determinations about the the output resistance, the resistance at the anode (r_a) must be calculated. This is typically found using information provided in the manufacturer provided datasheet in conjunction with the formula shown in equation 6.

$$r_a = \frac{\Delta V_a}{\Delta I_a} \quad (6)$$

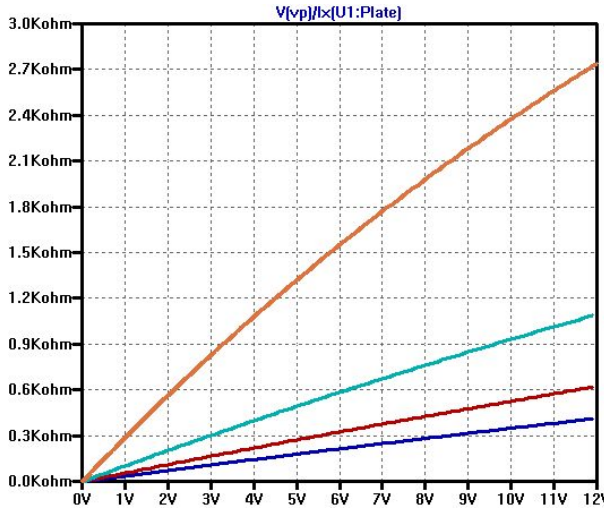
In the configuration shown in **Figure 4**, a 1 MΩ resistor connects the grid of the vacuum tube to ground putting 0 V on the grid. Since the cathode is connected to V_{EE} through R_2, the grid is positive with respect to the cathode. These devices were originally used with much higher voltages than most modern devices utilized today. With higher voltage ranges, it would be customary to use a load-line analysis to calculate r_a from the transfer characteristics given in the datasheet. Since this information lacks the precision necessary for low voltage operation, a plot of anode current vs. anode voltage was simulated in LTspice using the schematic shown in **Figure 11**.

***Figure 11**: 12AT7 Transfer Characteristic Schematic*



Since the grid voltage is positive with respect to the cathode, this puts the tube in a "saturation" mode similar to that of a bipolar transistor. Using LTspice and the model for the12AT7, a plot of r_a for grid voltages from 1 V to 4 V was generated and is shown in **Figure 12**. The orange line represents 1 V.

***Figure 12**: Plot of r_a with Applied Grid Voltages*



In order to get the full output swing of the input signal delivered to the load, the voltage at the cathode (V_k) should be as close to 0 V as possible. This however isn't possible since the tube would stop conducting well in the range according to the LTspice model data. Therefore, V_k was set to ~500 mV which gave us an estimated r_a of 3.6 kΩ. This also sets the Q-point of the tube to be roughly (1.8 mA, 6.5 V). With the remaining voltage, solving for R2 gives a value of 3 kΩ. At the point, enough information is known to solve for the output resistance of the voltage follower.

$$r_k = \frac{R_2 + r_a}{\mu + 1} \approx 108\ \Omega \qquad (7)$$

Figure 13 gives a logarithmic plot of the gain of the amplifier with the vacuum tube output stage using the previously found values. **Figure 14** shows the circuit with the vacuum tube mounted on the breadboard. The information shown in **Table 2** is a comparison table for the amplifier specification.

***Figure 13**: 12AT7 Class A with 100 Ω to 1 MΩ Load*

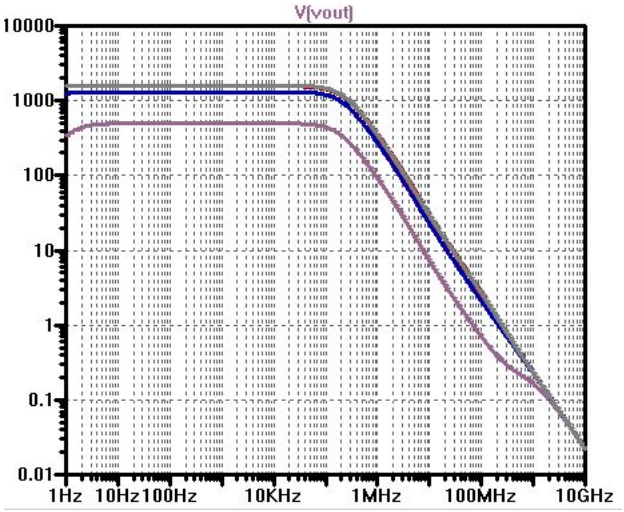


***Figure 14**: 12AT7 Class A with 100 Ω to 1 MΩ Load*

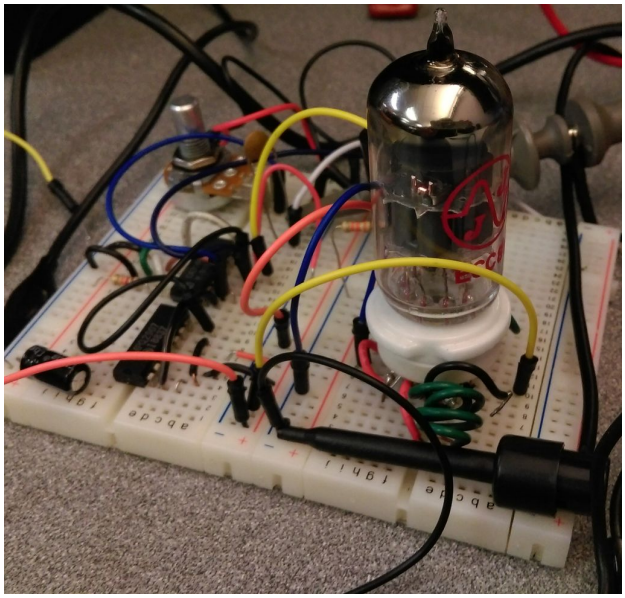
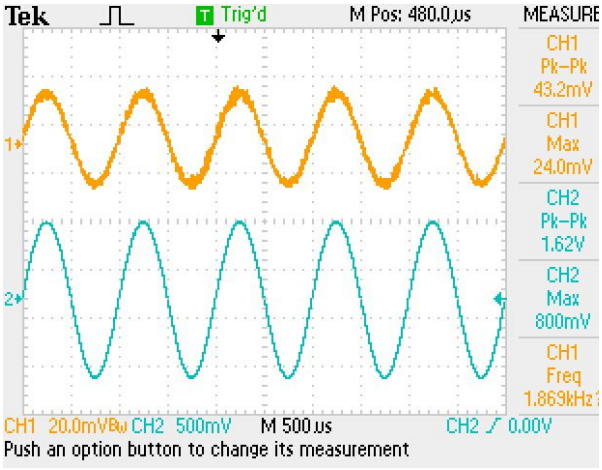


***Table 2**: Amplifier Specification Comparison VT Output*

Param	Hand	LT	Build	% Diff
$A_{v\ 12AT7}$	2000	1600	810	-59.5 %
$R_{in\ 12AT7}$	20 kΩ	14.6 kΩ	19.2 kΩ	-4.0 %
$R_{out\ 12AT7}$	108 Ω	231 Ω	740 Ω	5852 %

***Figure 15**: Output of Build with 12AT7 Output Stage*



IV. DISCUSSION

Part A: Effects of High Output Impedance

The results from the LTspice simulation weren't anything too terribly shocking. From previous work done, it was well understood that maximum power is transferred to a load when the output impedance of the circuit sourcing current for a load is equal to the impedance of the load itself. When the impedance of the load is larger than the output impedance, the most voltage is seen across the load. As the load impedance drops, the voltage seen at the output terminals lessens as more current becomes dissipated by the load. **Figure 5** shows that, when the load impedance is around 100 Ω, the gain of the amplifier is around 2. This is exactly what we found in the simulation.

Part B: Output Stage - Design and Simulation

The results from the simulation in Part B also follow the expected results. Taking the Early voltage and β from the LTspice models for our hand calculations at least indicates that similar models are at least being used. As expected with these parameters and setup, the BJT output stage had a higher output resistance than the NMOS stage largely due to its almost infinite input impedance. Using the value of K_n given in the model, the calculations are very within 34.7% to those predicted by the simulation.

Part C: Mini Op Amp - Build and Test

With the physical build, things start to get interesting. The first thing to note is the odd measurement shown of the oscilloscope input voltage shown in **Figure 9** and **Figure 10**. The oscilloscope seems to believe that this is ~20 mV when the DMM records ~2 mV. This must have been related to an internal setting regarding the attenuation on the oscilloscope probe, which was set for 10x. The menu settings for the channel showed that it expected that much attenuations, but something was wrong since it did not agree with the other measurements.

Secondly, the BJT stage's output impedance is about one tenth of what it should be, and the NMOS stage has a higher impedance that was expected. In conjunction, the gain of the amplifier with each stage is also considerably less. The output impedance of the differential amplifier stage was checked using the same method to calculate the voltage follower stages. It came out to be roughly 54 kΩ instead of the predicted 100 kΩ. Going under the assumption that the ro for the active load is the culprit, that would suggest that the CA3096 has an Early voltage of ~27.0 V. In all likeliness, this could just be due to a poorly setup model of the component. With a lower differential stage impedance, that would dramatically decrease the output resistance of the BJT stage. Lowering the Early voltage for the CA3096 did result in values much closer to those measured, but are not recorded in this paper.

The discrepancy in the output impedance of the NMOS stage is probably due to the K_n parameter of the BS170. In previous lab experiments, this K_n parameter has shown a good deal of fluctuation with varying drain currents. It's likely that a better suited NMOS would show considerable performance gain over this particular transistor. Further experimentation would be necessary to make a definitive determination.

Part D: Enhancing the Op Amp

Using a vacuum tube at low voltages is a far cry from an enhancement. However, using it for this experiment revealed some interesting aspects of how active devices cope with impedance in general. It was also interesting to see this device acts in the voltage follower configuration. Since the amplification factor is fixed for most practical purposes, triodes with high amplification factors have the lower output impedances. This is strikingly similar to the β of a BJT whereby the resistance seen on the base gets divided by this value from the viewpoint of the emitter. Though the fundamental principles in these two devices are radically different, it is surprising to see such a similar functionality show up in this application.

From the results in **Table 2**, it is apparent that there are some large discrepancies in how both LTspice and the hand calculations deal with the output resistance. More information regarding the theory behind the operation of vacuum tubes should undoubtedly be investigated. Being such an antiquated device, formidable resources on this topic were not easy to find. The interesting result while performing this part of the experiment was in the interaction between the grid and the anode. Without adding a resistor to the grid in an attempt to "anchor" it to the 0 V margin, the grid would appear largely negative. The output resistance and overall gain of the voltage follower stage improved considerably when the power supply rails were increase to ±12 V. This makes sense being that vacuum tubes typically operate at much higher voltages. Operating in ±6 V range most likely alters the small-signal models typically employed for design purposes.

V. CONCLUSIONS

This set of experiments revealed several interesting aspects and uses of the differential amplifier and how it is often used in the op amp configuration. The simulations and approximations used during design favored each other closely within a XX% . The measured results of the physical build, however, were drastically different. This really shows how crucial the transistor characteristics are when trying to design DC coupled circuits.

Additionally, comparisons between the different types of devices functioning as the output stage were examined. It seems that the 2N3904 emitter follower had the best overall performance in this circuit. This doesn't say anything definitive about BJTs in general, but it was an unexpected result given measured output impedance of the differential stage. The added mobility in the NPN over the NMOS does suggest a lower output impedance with this particular amount of current provided the resistance on the base is below a certain threshold and given a high β. When using any type of device for a voltage follower output stage, the most important considerations are using the right β, K_n, or μ to achieve the necessary impedance.

VI: APPENDICES

Appendix A: SPICE Model for CA3046

```
.MODEL CA3046    NPN(IS=10f BF=145.76 VAF=100
IKF=46.747m  ISE=114.23f  NE=1.483  BR=100.1m
VAR=100  IKR=10.01m  ISC=10f  RC=10  CJE=1.026p
MJE=333.33m CJC=991.79f MJC=333.33m TF=277.09p
XTF=309.38   VTF=16.364   ITF=1.7597   TR=10n)
VCEO=20 ICRATING=50m MFG=RCA)
```

Appendix B: SPICE Model for CA3096P

```
.MODEL CA3096P PNP(IS=10f BF=94.511 VAF=100
IKF=1.1177m ISE=976.47f NE=1.998 BR=100.1m
VAR=100 IKR=10.01m ISC=10f NK=532.43m
CJE=1.4535p MJE=333.33m CJC=3.8474p
MJC=333.33m TF=24.3n XTF=10.054 VTF=9.792
ITF=1.2571 TR=10n) VCEO=35 ICRATING=50m
MFG=RCA)
```

Appendix C: SPICE Model for 12AT7

```
.SUBCKT 12AU7A P G K
E1  2  0  VALUE={V(P,K)+18.28*V(G,K)}
R1  2  0  1.0K
Gp  P  K
VALUE={10.88E-6*(PWR(V(2),1.5)+PWRS(V(2),1.5))
/2}
Cgk G  K  1.6P
Cgp G  P  1.5P
Cpk P  K  0.5P
.ENDS 12AU7A
```